DMS LAB Limited

700V BiCDMOS process specification

› Description

- 700V 3.0um BiCDMOS process is DMS Lab Limited BCD high voltage technologies.

- Main target applications are analog switch ICs, AC-DC converters, driver ICs for applications using 400-700V supply. The typical breakdown voltage of the DMOS transistor is more than 700V and typical breakdown voltage of the HV NMOS transistor is more than 500V.

- Process combines power DMOS, HVNMOS, bipolar npn tratsistors, logic CMOS and as options HV CMOS processing steps to provide a wide variety of MOS and bipolar devices with different voltage levels on the same die.

- The 13 layers process module is available for 700V breakdown voltage of the DMOS. This process module provides locos insulation, single level poly, one level metal.

		Options
	Wafer	
1	**Well 1**	
2	**Well 2**	
3	**Active area**	
4	**Guard 1**	
5	**Guard 2**	
6	**Deep Drain**	
7	**P base**	
8	**Gate**	**P-drain**
9	**P+drain**	**N-drain**
10	**N+drain**	
11	**Contact**	
12	**Metal**	
13	**Passivation**	

- Advances in one chip process that integrate power IC's and power switch require the power devices with low power consumption, high breakdown voltage and high current driving capability. LDMOS (Lateral Double-diffused MOS) employing RESURF (REduced SURface Field) technology using low thickness of N- Well has allowed the construction of high voltage devices with low on-state resistance

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> Key Features

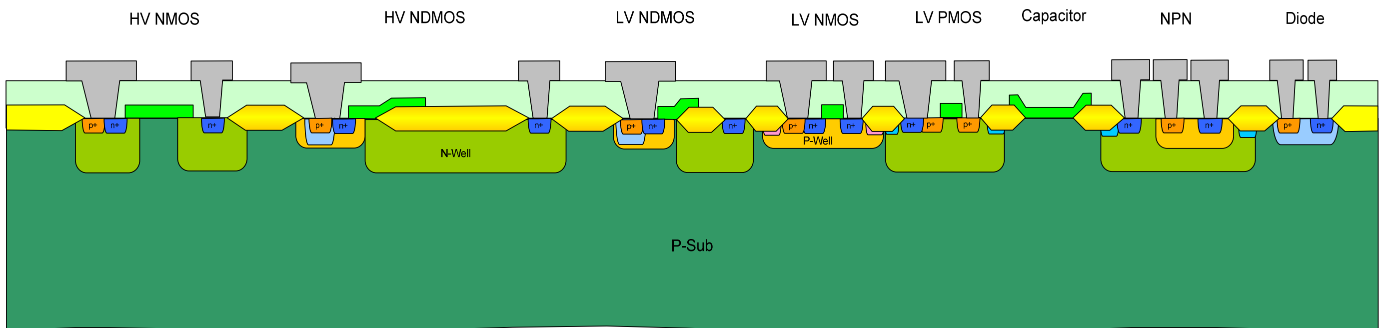
The power lateral NDMOS transistor with low Rdson and small area is the main HV component of the BiCDMOS 700V technology.

3.5um one poly, one metal, double Well BCD process.

A high number of different devices are available:

- 700V n-channel lateral power DMOS transistor
- 60V n-channel lateral DMOS transistor;
- 500V n-channel MOS transistor
- 12V n-channel MOS transistor;
- 12V p-channel MOS transistor;
- 20V n-channel MOS transistor; option
- 20V p-channel MOS transistor; option
- 25V NPN transistors;
- Zener diodes;
- Gate oxide capacitors;
- Low resistivity poly-Si resistors;
- Resistors in active layers.

> Schematic cross section



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> Basic design rules

Layer	Min width (um)	Min spacing (um)
Active Area (CMOS)	4.0	2.0
CMOS Gate	3.5	2.0
DMOS Gate	8.0	--
Contact	2.0	2.0
Metal-1	4.0	2.0
VIA	3.0	3.0
Metal-2	5.0	3.0

〉 Device Parameters of main elements for 700V process

ELEMENT	PARAMETER UNIT	SPEC MIN	SPEC MAX	MEASUREMENT CONDITIONS
HV LDMOS L=8.0 um, W=240 um	VTH, V	1.5	2.3	Id=0.1uA
	IDS, mA	35.0	-	Ug=Ud=10 V
	BVDS, V	700	-	Id=10uA
	Rsp, Ohm*mm2	-	24	Ug=10 V
	IDS, uA	-	50	Ug=Ub=Us=0 V, Ud =600 V
LV LDMOS L=8 um, W=50 um	VTH, V	1.5	2.3	Id=0.1uA
	IDS, mA	1.5	-	Ug=Ud=5 V
	BVDS, V	60	-	Id=10uA
HV NMOS L=35 um, W=1350 um	VTH, V	1.0	1.6	Id=0.1uA
	IDS, mA	40.0	-	Ug=Ud=10 V
	BVDS, V	500	-	Id=10uA
LV NMOS L=3.5 um, W=50 um	VTH, V	0.7	1.1	Id=0.1uA
	IDS, mA	2.5	3.5	Ug=Ud=5 V
	BVDS, V	12.0	-	Id=10uA
LV PMOS L=3.5 um, W=50 um	VTH, V	0.9	1.3	Id=0.1uA
	IDS, mA	1.5	2.5	Ug=Ud=5 V
	BVDS, V	12		Id=10uA
NPN Se=10x10 um2	BETA	50	150	Ib=10uA, Uc=1 V
	BVCE0, V	25	-	Ic=10uA, floating base
MV NMOS L=3.5 um, W=50 um	VTH, V	0.7	1.1	Id=0.1uA
	IDS, mA	2.0	3.0	Ug=Ud=5 V
	BVDS, V	20.0	-	Id=10uA
MV PMOS L=3.5 um, W=50 um	VTH, V	0.9	1.3	Id=0.1uA
	IDS, mA	0.5	1.5	Ug=Ud=5 V
	BVDS, V	20		Id=10uA
Diode	BV, V	9	-	Id=10uA
Zener Diode	BV, V	5.5	6.5	Id=10uA
Base Resistor	RS, Ohm/sq	550	650	Ir=10uA
PolySi- gate oxide – Well capacitor	Ccs, pF/um2	3,0E-4	4.0E-4	F=1MHz, Vmea=5V